What is claimed is:

1. A method of simulating a circuit having a hierarchical data structure, comprising:

partitioning the circuit into a plurality of group circuits, each group circuit includes one or more leaf circuits, wherein each leaf circuit produces a predictable set of output signals with a given set of input signals;

storing the group circuits in a scheduled event queue in accordance with priority in time which the group circuits need to be simulated;

retrieving from the scheduled event queue a set of group circuits for simulation within a predetermined time period;

distributing the set of group circuits into a set of predefined event lists, wherein each of the predefined event list stores one or more group circuits of a corresponding event type;

simulating the one or more group circuits in each of the predefined event list in accordance with a rate of change of signal conditions of each individual group circuit.

2. The method of claim 1, wherein the set of predefined event lists comprise:

an active event list for storing group circuits that need to be solved within the predetermined time period;

an isomorphic event list for storing group circuits that need to be solved due to changes in isomorphic behavior of leaf circuits in each of the group circuit; and

an adaptive event list for storing group circuits that need to be solved due to changes in connectivity between leaf circuits in each of the group circuit.

3. The method of claim 2, wherein the changes in isomorphic behavior include:

changes in isomorphic behavior detected at an output port of a leaf circuit;

changes in isomorphic behavior detected at an input port load of a corresponding leaf circuit; and

changes in isomorphic behavior detected at a port connectivity interface of a corresponding group circuit.

4. The method of claim 1, wherein each group circuit stores an event time for indicating priority in time the group circuit need to be solved, and wherein all leaf circuits in the corresponding group circuit share the same event time.

5. The method of claim 1, wherein the step of simulating comprises:

determining a global accepted time by selecting a maximum time among all local accepted times of the one or more group circuits;

determining a global current time by selecting a minimum time among all local current times of the one or more group circuits;

solving the one or more group circuits in accordance with the global accepted time and the global current time; and

storing solved group circuits to the scheduled event queue in response to the next event time the simulated group circuits need to be simulated.

6. The method of claim 5, wherein the local accepted time is the time of last accepted solution of a group circuit.

7. The method of claim 5, wherein the local current time is the time of a currently calculated solution of a group circuit.

8. The method of claim 5, wherein the local accepted time of a group circuit is less than the local current time of the corresponding group circuit.

9. The method of claim 5, wherein the global accepted time is less than the global current time.

10. The method of claim 1, wherein the step of simulating further comprises communicating a set of changes in signal conditions from a group circuit to other group circuits via a port connectivity interface.

11. The method of claim 10, wherein the port connectivity interface comprises:

a set of input vectors for referencing to a set of input ports of leaf circuits in receiver group circuits;

a set of output vectors for referencing to a set of output ports of leaf circuits in driver group circuits;

a set of load vectors for referencing to a set of loads of leaf circuits in the driver group circuits; and

an array of storage elements for storing information associating the set of loads to the set of input ports.

12. A system for simulating a circuit having a hierarchical data structure, comprising:

at least one processing unit for executing computer programs;

a user interface for performing at least one of the functions selected from the group consisting of entering a netlist representation of the circuit, viewing representations of the circuit on a display, and observing simulation results of the circuit;

a memory for storing a static database and a dynamic database of the circuit;

means for partitioning the circuit into a plurality of group circuits, each group circuit includes one or more leaf circuits, wherein each leaf circuit produces a predictable set of output signals with a given set of input signals;

means for storing the group circuits in a scheduled event queue in accordance with priority in time which the group circuits need to be simulated;

means for retrieving from the scheduled event queue a set of group circuits for simulation within a predetermined time period;

means for distributing the set of group circuits into a set of predefined event lists, wherein each of the predefined event list stores one or more group circuits of a corresponding event type;

means for simulating the one or more group circuits in each of the predefined event list in accordance with a rate of change of signal conditions of each individual group circuit.

13. The system of claim 12, wherein the set of predefined event lists comprise:

an active event list for storing group circuits that need to be solved within the predetermined time period;

an isomorphic event list for storing group circuits that need to be solved due to changes in isomorphic behavior of leaf circuits in each of the group circuit; and

an adaptive event list for storing group circuits that need to be solved due to changes in connectivity between leaf circuits in each of the group circuit.

14. The system of claim 13, wherein the changes in isomorphic behavior include:

changes in isomorphic behavior detected at an output port of a leaf circuit;

changes in isomorphic behavior detected at an input port load of a corresponding leaf circuit; and

changes in isomorphic behavior detected at a port connectivity interface of a corresponding group circuit.

15. The system of claim 12, wherein each group circuit stores an event time for indicating priority in time the group circuit need to be solved, and wherein all leaf circuits in the corresponding group circuit share the same event time.

16. The system of claim 12, wherein the means for simulating comprises:

means for determining a global accepted time by selecting a maximum time among all local accepted times of the one or more group circuits;

means for determining a global current time by selecting a minimum time among all local current times of the one or more group circuits;

means for solving the one or more group circuits in accordance with the global accepted time and the global current time; and

means for storing solved group circuits to the scheduled event queue in response to the next event time the simulated group circuits need to be simulated.

17. The system of claim 16, wherein the local accepted time is the time of last accepted solution of a group circuit.

18. The system of claim 16, wherein the local current time is the time of a currently calculated solution of a group circuit.

19. The system of claim 16, wherein the local accepted time of a group circuit is less than the local current time of the corresponding group circuit.

20. The system of claim 16, wherein the global accepted time is less than the global current time.

21. The system of claim 12, wherein the means for simulating further comprises means for communicating a set of changes in signal conditions from a group circuit to other group circuits via a port connectivity interface.

22. The system of claim 21, wherein the port connectivity interface comprises:

a set of input vectors for referencing to a set of input ports of leaf circuits in receiver group circuits;

a set of output vectors for referencing to a set of output ports of leaf circuits in driver group circuits;

a set of load vectors for referencing to a set of loads of leaf circuits in the driver group circuits; and

an array of storage elements for storing information associating the set of loads to the set of input ports.

23. A computer program product, comprising a medium storing computer programs for execution by one or more computer systems, the computer program product comprising:

a simulator module for simulating a circuit having a hierarchical data structure, wherein the simulator module is used in conjunction with at least a processing unit, a user

interface and a memory, and the simulator module includes one or more computer programs containing instructions for:

partitioning the circuit into a plurality of group circuits, each group circuit includes one or more leaf circuits, wherein each leaf circuit produces a predictable set of output signals with a given set of input signals;

storing the group circuits in a scheduled event queue in accordance with priority in time which the group circuits need to be simulated;

retrieving from the scheduled event queue a set of group circuits for simulation within a predetermined time period;

distributing the set of group circuits into a set of predefined event lists, wherein each of the predefined event list stores one or more group circuits of a corresponding event type;

simulating the one or more group circuits in each of the predefined event list in accordance with a rate of change of signal conditions of each individual group circuit.

24. The computer program product of claim 23, wherein the set of predefined event lists comprise:

an active event list for storing group circuits that need to be solved within the predetermined time period;

an isomorphic event list for storing group circuits that need to be solved due to changes in isomorphic behavior of leaf circuits in each of the group circuit; and

an adaptive event list for storing group circuits that need to be solved due to changes in connectivity between leaf circuits in each of the group circuit.

25. The computer program product of claim 24, wherein the changes in isomorphic behavior include:

changes in isomorphic behavior detected at an output port of a leaf circuit;

changes in isomorphic behavior detected at an input port load of a corresponding leaf circuit; and

changes in isomorphic behavior detected at a port connectivity interface of a corresponding group circuit.

26. The computer program product of claim 23, wherein each group circuit stores an event time for indicating priority in time the group circuit need to be solved, and wherein all leaf circuits in the corresponding group circuit share the same event time.

27. The computer program product of claim 23, wherein the instructions for simulating comprises:

determining a global accepted time by selecting a maximum time among all local accepted times of the one or more group circuits;

determining a global current time by selecting a minimum time among all local current times of the one or more group circuits;

solving the one or more group circuits in accordance with the global accepted time and the global current time; and

storing solved group circuits to the scheduled event queue in response to the next event time the simulated group circuits need to be simulated.

28. The computer program product of claim 27, wherein the local accepted time is the time of last accepted solution of a group circuit.

29. The computer program product of claim 27, wherein the local current time is the time of a currently calculated solution of a group circuit.

30. The computer program product of claim 27, wherein the local accepted time of a group circuit is less than the local current time of the corresponding group circuit.

31. The computer program product of claim 27, wherein the global accepted time is less than the global current time.

32. The computer program product of claim 23, wherein the instructions for simulating further comprises instructions for communicating a set of changes in signal conditions from a group circuit to other group circuits via a port connectivity interface.

33. The computer program product of claim 32, wherein the port connectivity interface comprises:

a set of input vectors for referencing to a set of input ports of leaf circuits in receiver group circuits;

a set of output vectors for referencing to a set of output ports of leaf circuits in driver group circuits;

a set of load vectors for referencing to a set of loads of leaf circuits in the driver group circuits; and

an array of storage elements for storing information associating the set of loads to the set of input ports.